Amendments to the Specification

Please replace the paragraph at Page 1, lines 3-5, with the following amended paragraph:

The invention relates to methods of making ~~an~~ atomic integrated circuit devices and more particularly to methods of making improved, miniaturized atomic semiconductor integrated circuit devices.

Please replace the paragraph at Page 2, lines 5-12, with the following amended paragraph:

According to Peltzer's patent, the Fairchild's Isoplanar device 40 as typified by ~~Fig. 4~~ Fig. 1 in his '125 patent has a n-type epitaxial silicon layer 42 formed on a p-type substrate 41. Oxide isolating regions, e.g., 44a, 44b, 44c and 44d ~~were~~ are used to isolate the different components. Each of these oxide isolating regions has a wide central flat bottom each occupying much of the chip real estate and producing unnecessarily larger devices.

Please replace the paragraph at Page 2, line 26 to Page 3, line 8 with the following amended paragraph:

Specifically, the rounded groove 21 produces a curved, exposed peripheral junction surface ~~is~~ thereby preventing contamination by rubbing contacts with dust particles. Such contacts form, e.g., metallic shorting paths and drastically reduce the device yield by increasing leakage current and decreasing breakdown voltage. Li's 3,430,109 patent discloses at column 5, lines 15-20 that for a one-micron (thick) PN

junction region, a single-atomic gold chain one-micron long contains 3,903 gold atoms giving a leakage current of 0.15 ma at 50 volts thereby destroying the device. A single 1-micron gold particle could possibly destroy 7.977 $x10^6$ devices.

Please replace the paragraph at Page 17, lines 7-9 with the following amended paragraph:

Fig. 2 shows partial vertical cross-section of Li's prior-art isoplanar device with a round-bottomed and sloping sided isolating groove of zero width;

Please replace the paragraph at Page 23, line 26 to Page 24, line 8 with the following amended paragraph:

As shown above, an ideally intrinsic silicon material is an insulator. Depending on its purity, a practical intrinsic silicon material can be sufficiently electrically insulating, in comparison to or when used in combination with the p-type "silicon" substrate and n-type "silicon" pockets, to form the gate or field oxide layers of a practically useful MOS or CIS device. As will be shown shortly, such ~~as~~ an intrinsic silicon MOS or CIS device is, at least as to environmental resistance, distinctly better than the conventional MOS or CIS devices, even though they may be less pure and, thereby electrically more leaky.

Please replace the paragraph at Page 25, lines 3-16 with the following amended paragraph:

In the device of 3a, the downward diffusion of the n-type dopant from the grooved, top cylindrical surface forms in the

inert or intrinsic silicon material 31 a generally cylindrical n-type diffusional front (ndf) 35. This diffusional front is generally concentric with the cylindrical grooved surface 32, according to the laws of diffusion. The upward diffusion of the p-type dopant from the planar bottom major surface 34 of the intrinsic wafer 31 forms a generally horizontal and planar p-type diffusional front (pdf) 36. The PN junction region 37 must from where n-type and p-type dopant concentrations ~~is~~ in the wafer is substantially equal, below the generally planar p-type diffusional front but above the generally cylindrical n-type diffusional front.

Please replace the paragraph at Page 26, line 25 to Page 27, line 10 with the following amended paragraph:

In a preferred embodiment for making the new gate layer of this invention, a laser system is used. The integrated device of Fig. 4 has a p-type silicon substrate 41, on which there are adjacent but laterally spaced-apart n-type silicon pockets 42. PN junction regions ~~43~~ are formed where the n-type semiconductor pockets 42 contact the p-type substrate 41. The adjacent silicon pockets 42, respectively, a source and a drain region~~s~~, are laterally spaced apart by a gap of a prespecified gate length (e.g., 0.001-0.1 microns) on a top surface of the substrate in the gate area. For extreme dynamic resistance, both the substrate 41 and pockets 42 may be nearly intrinsic silicon material, respectively slightly p- and n-type doped. The gate area has a length roughly the same as, but slightly greater than, the prespecified gate length to minimize leakage.

Please replace the paragraph at Page 30, lines 5-16 with the following amended paragraph:

According to this atomic model, an atomic chain or sheet a few angstroms in diameter or thickness for silicon can easily bend or flex enough to accommodate any thermal mismatch strain. The bending occurs when one or both atoms simply rotate around its neighbor without changing the distance therebetween. There is therefore no work done or energy consumed, since both the repulsive and attractive forces depend only the interatomic distance, which is constant before and after the bending. Nor are there any gain or loss of energy, due to either the attractive force ~~of~~ or the repulsive force component. This has been observed even in "brittle materials such as oxide ceramics, e.g., SiO_2.

Please replace the paragraph at Page 31, lines 8-16 with the following amended paragraph:

An embodiment of the Fig. 6 device comprises a chain or sheet of mixed doped silicon atoms 66 (hatched) and insulating materials such as intrinsic silicon atoms or oxide/nitride molecules 65 (in white). Dopants for the hatched semiconducting silicon atoms 66 include n-type dopant P and Sb, and p-type Al and B. These chains or sheets of semiconducting and insulating atoms (or molecules) 62, 63, 64 and ~~64~~ 65 are embedded in p-type semiconducting layers 62 and 64, and n-type semiconducting layers 63 and 65.

Please replace the paragraph at Page 31, line 26 to Page 32, line 6 with the following amended paragraph:

Consider the simplest atomic silicon chain 61, if the special impurity atom or molecule 66 differs in resistivity

values from the other atoms ~~65~~ 69 in the chain or sheet by one or two orders of magnitude, or is metal-like or semiconductor-like, a new thin-film solid-state device or circuit then results, with film layer thicknesses ranging from several submicrons down to several or even one atomic thickness. Such device may be a single-electron, single-hole, single-carrier, or single-photon device, for reasons shown below.

Please replace the paragraph at Page 32, lines 6-12 with the following amended paragraph:

In a preferred embodiment of the Fig. 6 device, the entire atomic chain or sheet 61, 61', or 61'' is only one-half micron through several atomic layers to even one single atomic layer wide or thick. This chain is mostly of unhatched intrinsic silicon atoms or oxide/nitride molecules ~~65~~ 69, but still has some hatched atoms of, e.g., P, Sb, Al, or B-doped silicon (66). The unhatched part, if perfect, forms a good insulating wall.

Please replace the paragraph at Page 32, lines 19-26 with the following amended paragraph:

For example, as shown in Fig. 6, any n-type doped semiconductor atom 66 with five electrons on each atom present on the chain 61 will join the n-type semiconductor material region 63 to become part thereof. The intrinsic silicon atoms or oxide molecules ~~65~~ 69 for the isolating wall 61 electrically isolates the left p-side 62 from the right n-side 63, except where the impurity-doped semiconductor atom or molecule 66 is located forming thereat an atomic PN junction and a selected leakage or drift path.

Please replace the paragraph at Page 32, line 27 to Page 33, line 4 with the following amended paragraph:

The p-type region 62 has an external positive electrode 67 at the bottom of the semiconductor region 62 and an external negative electrode 68 at the top. The n-type region 63 has a negative electrode 67' at the front, and a positive electrode 68 at the rear. An external electrical field is thus produced in the region 63 causing the holes to drift toward the front of the region 63, and the electrons toward the rear in the same region.

Please replace the paragraph at Page 33, lines 5-14 with the following amended paragraph:

When a light beam, such as from a laser beam, shines on the p-type material region 62 in Fig. 6, an electron-hole pair of carriers is locally generated in the region due to photon injection from, e.g., a laser diode beam. A laser diode can produce a ray of light at a precise wavelength and can modulate the amplitude of the light at very high frequencies without distortion by using a special optical fiber capable of lazing at the same wavelength. An optical array of laser diodes emits multiple laser beams useful in, e.g., an optical communication system. The device of Fig. 6 then can form, e.g., an optical reader.

Please replace the paragraph at Page 33, line 21 to Page 34, line 7 with the following amended paragraph:

The freed hole from the electron-hole pair in Fig. 6 will then: a) drift vertically upward ~~or downward~~ through the field 67-68 to the nearest n-type impurity atom 66 and the associated

PN junction field; b) be pushed rightward by the PN junction field into the n-type semiconductor region 63; c) instantly recombines with an electron in the electron-dominant n-type semiconductor region 63; and d) causes the back negative electrode 67′ to supply an electron needed by the region 63 to maintain its charge neutrality, creating a second electrical signal.

Please replace the paragraph at Page 34, line 27 to Page 35, line 6 with the following amended paragraph:

Decreasing the thickness of the p-type layer 62 and lower the light aiming point on region 62 in the device of Fig. 6 increases the sensitivity and reduces the delay time of the first electrical signal after the laser injection. Maximum sensitivity and minimum delay time of the first electrical signal in region 62 are obtained with minimum thickness of the p-type semiconductor layer 62, which is shown as continuous white vertical area in Fig. 6 but actually is filled with one to several or more columns of the insulating ~~semiconductor atoms 65~~ atoms or molecules 69.

Please replace the paragraph at Page 34, lines 8-19 with the following amended paragraph:

The externally applied electrical fields from the external electrode pairs 67-68 and 67′-68′, and the mobilities of holes and electrons in semiconductor silicon are known. The distances of carrier travels are related to the designed device structure of the insulating atoms ~~65~~ 69 and the specified distribution of the dope semiconductor atoms 66 on the chain or sheet 61. Hence, the first electrical signal representing replenishing the

lost hole in the p-type semiconductor region 62 and the second electrical signal representing replenishing the lost electron in the n-type region 63 have predictable time delays after the laser photon impacts on the device to generate the electron-hole pair.

Please replace the paragraph at Page 41, lines 10-28 with the following amended paragraph:

The insulating chain or panel 61, 61', 61'', ...may not be atomic but have appreciable width in a direction normally of the paper in Fig. 6, and also in depths extending horizontally toward the back of the paper so that single impurity-doped atom 66 now are semiconductor regions of substantial sizes. On the other hand, each of the semiconductor regions 62, 63, 64, 65, ... may be only single atomic layers of p-type or n-type semiconductor material. Ion-implanted or atomic tweezer-picked chains or arrays of insulating material atoms ~~65~~ 69 and dope atoms 66 may form the required single atomic layers 61, 61', 61'',... Ass shown above, atomic layers of various materials have been formed. The semiconductor regions, reduced to single atomic layers, may even be reduced in widths to be single atoms wide. The solid optoelectric device then reaches an ultimate miniaturization. Still, the performance of the individual components will remain unaffected. The atomic tweezer-formed semiconductor lines or regions 62, 63, 64, and 65, together with the mixed insulator and doped semiconductor chains 61, 61', 61'',... form light-sensing or light-detecting ~~deices~~ devices possibly only three or four atoms wide.

Please replace the paragraph at Page 56, lines 17-29 with the following amended paragraph:

The laser beam can be focused to such a beam size with such a power density profile to remove a selected part of the melt materials by material ejection or evaporation thereby forming a concave depression containing the remaining melt material. Rapid or splat cooling of the remaining molten gate material produces ultra-fine solidifying grains or subgrains further smoothing the lower gate layer surface. In addition, progressively solidifying the melt material from the bottom up purifies the solidifying ~~the~~ melt material, according to the relevant phase diagram of the gate layer material. The most material purification occurs precisely at the lowest or first-to-freeze layer closest to the substrate to thereby having the best gate material properties including the highest electrical insulation properties thereat.

Please replace the paragraph at Page 72, line 24 to Page 73, line 7 with the following amended paragraph:

The insulating chain or panel 61, 61', 61'', ... may not be atomic buy have appreciable width in a direction normally of the paper in Fig. 6, and also in depths extending horizontally toward the back of the paper so that single impurity-doped atom 66 now are semiconductor regions of substantial sizes. On the other hand, each of the semiconductor regions 62, 63, 64, 65, ... may be only single atomic layers of p-type or n-type semiconductor material. Ion-implanted or atomic tweezer-picked chains or arrays of insulating material atoms ~~65~~ 69 and dope atoms 66 may form the required single atomic layers 61, 61', 61'', ... As shown above, atomic layers of various materials have been formed. The semiconductor regions, reduced to single

atomic layers, may even be reduced in widths to be single atoms wide.